OpenCL編譯器與課程論壇

Fusion System Architecture and Heterogeneous Computing Programming

時間：100年12月21日（星期三）, 09:00~15:30
地點：國立清華大學第二綜合大樓8F 國際會議廳

Time	Session	Agenda	
09:00-09:25	**Registration**		
09:25-09:30	**Opening**		
09:30-10:45	Session 1	• **Fusion System Architecture** • **Heterogeneous Computing Programming** o OpenCL, Cuda, Renderscript	
10:45-11:00	**Break**		
11:00-12:15	Session 2	• **Heterogeneous Computing Programming** o C++ AMP o Trends in Heterogeneous Computing Programming ▪ C++11 highlights ▪ Memory model • **Research Opportunities for Heterogeneous Computing**	
12:15-12:30	**Q&A**		
12:30-14:00	**Lunch**		
14:00-15:00	嵌入式多核心程式語言	中華資工系	許慶賢 教授
		靜宜資工系	李冠憬 教授
		中正資訊工程系	陳鵬升 教授
		交大資訊工程系	游逸平 教授
		台科大資工系	黃元欣 教授
15:00~15:30	**Discussion**		

Speaker's Bio:

Roy D.C. Ju has been a compiler architect and a Fellow at Advanced Micro Devices since 2006. He has been driving the optimization technology for high-performance, cross-platform compilation for AMD multi-core CPU and GPU architectures. He is currently the compiler architect for the Fusion System Architecture project. Prior to joining AMD, he made a brief stop at Google Inc. working on a distributed system and Google Desktop. From 1999 to 2005, he was a senior researcher and the manager of Compiler Technology group at the Programming System Lab in the Microprocessor Technology Labs, Intel Corp. He led an effort in innovating programming and compiler technology for multi-core architectures, including a multi-core network processor. He had been the architect of an IA-64 open source research compiler (Open Research Compiler), which provided an infrastructure for compiler and architecture research on IA-64 to the research and open source communities. He was with the Hewlett-Packard Company from 1994 to 1999, where he was a project lead in designing and developing an optimizing compiler for IA-64. He worked at IBM from 1992 to 1994 in developing a then state-of-the-art Fortran 90 optimizing compiler. His primary research interests include compiler optimizations, optimization for memory hierarchy, program analysis, computer architecture, multi-core systems, and parallel processing. He received his B.S. in Electrical Engineering from National Taiwan University in 1984. He received his M.S. and Ph.D. in Electrical and Computer Engineering from the University of Texas at Austin in 1988 and 1992, respectively. He currently holds 24 U.S. patents and has published more than 60 journal and conference papers in various areas, including array language optimizations, compilation for instruction-level parallelism, cache optimization, coarse-grained parallelization, etc. He has served on the program committees of a number of conferences, such as MICRO-33, MICRO-35, PLDI '01, MSP '02, CGO '03, '04, '05, LCTES '05, COCV '05, Open64 Workshop '08 and '09, EUC '09 and '10, PPoPP '11, and PACT'11. He was a General Co-Chair of CGO '07.

主辦單位：教育部前瞻晶片系統設計人才培育先導計畫嵌入式軟體聯盟（ESW）　協辦單位：經濟部學界科專「嵌入式異質多核心系統技術研發計劃」
國立清華大學資訊工程學系