104 年 05 月　通過 學術審查

年　　級：博七 (92 入學)

著作列表

Journal Papers

- **Chung-Ju Wu**, Chia-Han Lu, and Jenq Kuen Lee, "Register Spilling via Transformed Interference Equations for PAC DSP Architecture", *Concurrency and Computation: Practice and Experience*, Volume 26, Issue 3, pp. 779-799, 10 March 2014.
- **Chung-Ju Wu**, Yu-Te Lin, and Jenq Kuen Lee, "Instruction Scheduling Methods and Phase Ordering Framework for VLIW DSP Processors with Distributed Register Files", *Journal of Supercomputing*, Volume 61, Issue 3, pp. 1024-1047, September 2012.
- Chih-Wei Chang, Tay-Jyi Lin, **Chung-Ju Wu**, Jenq Kuen Lee, Yuan-Hua Chu, and An-Yeu Wu, "Parallel Architecture Core (PAC) - the First Multicore Application Processor SoC in Taiwan Part I: Hardware Architecture & Software Development Tools", *Journal of Signal Processing Systems*, Volume 62, Issue 3, pp. 373-382, March 2011.
- Chia-Han Lu, Wen-Li Shih, **Chung-Ju Wu**, and Jenq Kuen Lee, "Achieving spilling-friendly register file assignment for highly distributed register files", *Journal of Supercomputing*, Volume 69, Issue 3, pp. 1342-1362, September 2014.

Conference Papers

- **Chung-Ju Wu**, Chia-Han Lu, and Jenq Kuen Lee, "Expression Rematerialization for VLIW DSP Processors with Distributed Register File", *Compilers for Parallel Computers*, Zurich, Switzerland, January 2009.
- **Chung-Ju Wu**, Sheng-Yuan Chen, and Jenq Kuen Lee, "Copy Propagation Optimizations for VLIW DSP Processors with Distributed Register Files", *Languages and Compilers for Parallel Computing*, New Orleans, USA, November 2006.

Conference Posters

- **Chung-Ju Wu** and Jenq Kuen Lee, "Compiler Frameworks for Embedded VLIW DSP Processors", *Languages, Compilers, and Tools for Embedded Systems*, Chicago (ACM LCTES), USA, June 2005.

Patents

- **Chung-Ju Wu**, Yu-Te Lin, Jenq Kuen Lee, "Method for allocating registers for a processor based on cycle information",
  - US Grant Patent,
  - Publication number: US8539462 B2,
  - Publication date: Sep 17, 2013.
- Chia-Han Lu, **Chung-Ju Wu**, Yu-Te Lin, Jenq Kuen Lee, "Spilling method involving register files based on communication costs and use ratio",
  - US Grant Patent,
  - Publication number: US8510539 B2,
  - Publication date: Aug 13, 2013.
- Jenq Kuen Lee, **Chung-Ju Wu**, Sheng-Yuan Chen, "Method for copy propagations for a processor with distributed register file design",
  - US Grant Patent,
  - Publication number: US8051411 B2,
  - Publication date: Nov 1, 2011.

GCC Contribution

- **Chung-Ju Wu** and Shiva Chen, "Contributing new target port: Andes nds32", *gcc-patches@gcc.gnu.org*, GCC community, July 2013.

104 年 05 月　通過 學術審查

年　　級：博七　(97 入學)

著作列表

Journal Papers

1. **Seong-I Lei** and Wai-Kei Mak, "Simultaneous Constrained Pin Assignment and Escape Routing Considering Differential Pairs for FPGA-PCB Co-design," IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, vol. 32, no. 12, pp. 1866-1878, Dec. 2013.

Conference Papers

1. **Seong-I Lei**, Chris Chu and Wai-Kei Mak, "Double Patterning-Aware Detailed Routing with Mask Usage Balancing," International Symposium on Quality Electronic Design, Santa Clara, USA, pp. 219-223, 2014.

2. **Seong-I Lei** and Wai-Kei Mak, "Simultaneous Constrained Pin Assignment and Escape Routing for FPGA-PCB Codesign," International Conference on Field Programmable Logic and Applications, Chania, Greece, pp. 435-440, 2011. **(citation number = 2)**

3. **Seong-I Lei** and Wai-Kei Mak, "Maze Routing with Minimum Cost Buffer Insertion under Slew and Obstacle Constraints," The 20th VLSI Design/CAD Symposium, Hualien, Taiwan, 2009.

In progress of submission

1. **Seong-I Lei** and Wai-Kei Mak, "Optimizing Pin Assignment and Escape Routing for Blind-Via-Based PCBs," submitted to IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS. (under major revision)

104 年 05 月　通過 學術審查

年　　級：博六　(98 入學)

著作列表

Journal Papers

1. **Hsi-An Chien**, Ye-Hong Chen, Szu-Yuan Han, Hsiu-Yu Lai, and Ting-Chi Wang, "On Refining Row-Based Detailed Placement for Triple Patterning Lithography," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (*TCAD*), vol. 34, no. 3, pp. 778-793, March 2015.

Conference Papers

1. **Hsi-An Chien**, Szu-Yuan Han, Ye-Hong Chen, and Ting-Chi Wang, "A Cell-Based Row-Structure Layout Decomposer for Triple Patterning Lithography," in *Proceedings of International Symposium on Physical Design* (*ISPD*), pp. 67-74, Monterey, CA, USA, March 2015.

2. **Hsi-An Chien**, Zhen-Yu Peng, Yun-Ru Wu, Ting-Hsiung Wang, Hsin-Chang Lin, Chi-Feng Wu, and Ting-Chi Wang, "Mask-Cost-Aware ECO Routing," in *Proceedings of Design, Automation & Test in Europe Conference & Exhibition* (*DATE*), pp. 1-4, Dresden, Germany, March 2014.

3. **Hsi-An Chien** and Ting-Chi Wang, "Redundant-Via-Aware ECO Routing," in *Proceedings of Asia and South Pacific Design Automation Conference* (*ASP-DAC*), pp. 418-423, Suntec, Singapore, January 2014.

104 年 05 月　通過 學術審查

年　　級：博 六 （97 碩入，98 下直升）

著作列表

Journal Papers

1. **H.M. Chou**, M.Y. Hsiao, Y. C. Chen, K. H. Yang, J. Tsao, and S.C. Chang, W. B. Jone, and T. F. Chen, "Soft-Error Tolerant Design Methodology for Balancing Performance Power and Reliability," *IEEE Trans. Very Large Scale Integration Systems (TVLSI)*, 2014. (Impact Factor: 1.142)

2. **H.M. Chou**, Y. C. Chen, J. Tsao, K. H. Yang, S.C. Chang, W. B. Jone, and T. F. Chen "High-Performance Deadlock-Free ID Assignment for Advanced Interconnect Architecture," *IEEE Trans. Very Large Scale Integration Systems (TVLSI)*, 2015. (Impact Factor: 1.142)

Conference Papers

1. Y.C. Kao, **H.M. Chou**, K.T. Tsai, and S.C. Chang, "An Efficient Phase Detector Connection Structure for the Skew Synchronization System," in *Proc. Design Automation Conference (DAC)*, 2010. (Citations: 4)

2. Y.C. Kao, **H.M. Chou**, K.T. Tsai, and S.C. Chang, "Synthesis of an Efficient Controlling Structure for Post-Silicon Clock Skew Minimization," in *Proc. International Conference on Computer Aided Design (ICCAD)*, 2010. (Citations: 4)

3. **H.M. Chou**, H. Yu, and S.C. Chang, "Useful-Skew Clock Optimization for Multi-Power Mode Designs," in *Proc. International Conference on Computer Aided Design (ICCAD)*, 2011. (Citations: 4)

4. Y.C. Kao, K.T. Tsai, **H.M. Chou**, and S.C. Chang, "Post Silicon Skew Tuning: Survey and Analysis," in *Proc. Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2012.

5. H.Y. Lin, C.Y. Wang, S.C. Chang, Y.C. Chen, **H.M. Chao**, C.Y. Huang, Y.C. Yang, and C.C. Shen, "A Probabilistic Analysis Method for Functional Qualification under Mutation Analysis," in *Proc. Design, Automation & Test in Europe Conference & Exhibition (DATE)*, 2012. (Citations: 4)

6. **H.M. Chou**, H. C. Wu, Y. C. Chen, and S.C. Chang "Concurrency-Oriented SoC Re-Certification by Reusing Block-Level Test Vectors," in *Proc. International Symposium on Quality Electronic Design (ISQED)*, 2014.

7. **H.M. Chou**, H. C. Wu, Y. C. Chen, J. Tsao, and S.C. Chang "Hybrid Coverage Assertions for Efficient Coverage Analysis across Simulation and Emulation Environments," in *Proc. Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2015.